

IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) A method of replacing standard cells with high speed cells in ~~[[the]]~~ a design of a circuit using a computer program, said ~~application-specific integrated~~ circuit design comprising a plurality of high speed cells and a plurality of standard cells, said high speed cells and said standard cells being arranged to form a plurality of paths ~~on said application-specific integrated circuit~~, said method comprising the steps of:

timing said plurality of paths;

identifying cells occurring on paths for which timing targets are not met, the paths for which timing targets are not met belonging to a first set of paths; and

upgrading at least one of said identified cells to a high speed cell;

wherein the first set of paths is determined from a second set of paths, and the second set of paths is changed to include an increased number of paths if the paths for which timing targets are not met number less than a specified number of paths.

2. (Currently Amended) A method as claimed in claim 1, further comprising the step of determining ~~[[a]]~~ the first set of paths, ~~wherein said step of identifying cells occurring on paths for which timing targets are not met is performed on paths belonging to the first set of paths.~~

3. (Currently Amended) A method according to claim [[2]] 1 wherein said first set of paths is a set of paths that have [[the]] slowest timings.

4. (Currently Amended) A method according to claim [[2]] 1 wherein the ~~first set~~ specified number of paths comprises a predetermined number of paths.

5. (Currently Amended) A method as claimed in claim [[2]] 1 wherein the first set of paths are ordered according to timing and allocated an order number.

6. (Currently Amended) A method as claimed in claim 1 wherein the cells identified as occurring on said set of paths for which timing targets are not met are ranked in order of [[the]] a contribution of the cell to [[the]] a timing of a path.

7. (Currently Amended) A method as claimed in claim 6 wherein the contribution of the cell to the timing of the path is calculated using at least one of:

[[the]] an order number of each path the cell occurs on; and
a transition time of the cell.

8. (Currently Amended) A method as claimed in claim 6 wherein a predetermined number of [[the]] highest ranked cells are replaced with high speed cells.

9. (Currently Amended) A method as claimed in claim ~~[[2]]~~ 1 wherein the first set of paths comprises paths that each begin at one of a plurality of inputs and terminate at one of a plurality of ~~first~~ registers.

10. (Currently Amended) A method as claimed in claim ~~[[2]]~~ 1 wherein the first set of paths comprises paths that each begin at one of ~~[[the]]~~ a plurality of first registers and terminate at one of a plurality of second registers.

11. (Currently Amended) A method as claimed in claim ~~[[2]]~~ 1 wherein the first set of paths comprises paths that each begin at one of ~~[[the]]~~ a plurality of ~~second~~ registers and terminate at one of a plurality of outputs.

12. (Cancelled).

13. (Currently Amended) A method as claimed in claim 1 wherein the ~~application specific integrated~~ circuit design comprises a plurality of ~~end-points~~ endpoints at which the plurality of paths terminate.

14. (Currently Amended) A method as claimed in claim 13 wherein the ~~end points~~ endpoints are cells.

15. (Currently Amended) A method as claimed in claim ~~[[12]]~~ 13 wherein the second set of paths comprises one path per endpoint.

16. (Currently Amended) A method as claimed in claim ~~[[12]]~~ 13 wherein the second set of paths comprises a plurality of paths per endpoint.

17. (Currently Amended) A method as claimed in claim 13 wherein the second set of paths is changed to comprise an increased number of paths per endpoint ~~if the number of paths in the first set of paths is greater than the number of paths for which timing targets are not met.~~

18. (Original) A method as claimed in claim 1 wherein the circuit is an integrated circuit.

19. (Original) A method as claimed in claim 18 wherein the integrated circuit is an application specific integrated circuit.

20. (Currently Amended) A computer program for replacing standard cells with high speed cells in ~~[[the]]~~ a design of a circuit, said ~~application-specific-integrated~~ circuit design comprising a plurality of high speed cells and a plurality standard cells, said high speed cells and said standard cells being arranged to form a plurality of paths ~~on said application specific-integrated-circuit~~, said computer program arranged to carry out the steps of:

timing said plurality of paths;

identifying cells occurring on paths for which timing targets are not met, the paths for which timing targets are not met belonging to a first set of paths; and

upgrading at least one of said identified cells to a high speed cell;

wherein the first set of paths is determined from a second set of paths, and the second set of paths is changed to include an increased number of paths if the paths for which timing targets are not met number less than a specified number of paths.

21. (Currently Amended) A computer program as claimed in claim 20, further arranged to carry out the step of determining ~~[[a]]~~ the first set of paths ~~; wherein said step of identifying cells occurring on paths for which timing targets are not met is performed on paths belonging to the first set of paths.~~

22. (Currently Amended) A computer program according to claim ~~[[21]]~~ 20 wherein said first set of paths is a set of paths that have ~~[[the]]~~ slowest timings.

23. (Currently Amended) A computer program according to claim ~~[[21]]~~ 20 wherein the ~~first set~~ specified number of paths comprises a predetermined number of paths.

24. (Currently Amended) A computer program as claimed in claim ~~[[21]]~~ 20 wherein the first set of paths are ordered according to timing and allocated an order number.

25. (Currently Amended) A computer program as claimed in claim 20 wherein the cells identified as occurring on said set of paths for which timing targets are not met are ranked in order of ~~[[the]]~~ a contribution of the cell to ~~[[the]]~~ a timing of a path.

26. (Currently Amended) A computer program as claimed in claim 25 wherein the contribution of the cell to the timing of the path is calculated using at least one of:
~~[[the]]~~ an order number of each path the cell occurs on; and
a transition time of the cell.

27. (Currently Amended) A computer as claimed in claim 25 wherein a predetermined number of ~~[[the]]~~ highest ranked cells are replaced with high speed cells.

28. (Currently Amended) A computer program as claimed in claim ~~[[21]]~~ 20 wherein the first set of paths comprises paths that each begin at one of a plurality of inputs and terminate at one of a plurality of ~~first~~ registers.

29. (Currently Amended) A computer program as claimed in claim ~~[[21]]~~ 20 wherein the first set of paths comprises paths that each begin at one of ~~[[the]]~~ a plurality of first registers and terminate at one of a plurality of second registers.

30. (Currently Amended) A computer program as claimed in claim ~~[[21]]~~ 20 wherein the first set of paths comprises paths that each begin at one of ~~[[the]]~~ a plurality of ~~second~~ registers and terminate at one of a plurality of outputs.

31. (Cancelled).

32. (Currently Amended) A computer program as claimed in claim 20 wherein the ~~application-specific-integrated~~ circuit design comprises a plurality of ~~end-points~~ endpoints at which the plurality of paths terminate.

33. (Currently Amended) A computer program as claimed in claim 32 wherein the ~~end-points~~ endpoints are cells.

34. (Currently Amended) A computer program as claimed in claim ~~[[31]]~~ 32 wherein the second set of paths comprises one path per endpoint.

35. (Currently Amended) A computer program as claimed in claim ~~[[31]]~~ 32 wherein the second set of paths comprises a plurality of paths per endpoint.

36. (Currently Amended) A computer program as claimed in claim 32 wherein the second set of paths is changed to comprise an increased number of paths per endpoint ~~if the number of paths in the first set of paths is greater than the number of paths for which timing targets are not met.~~

37. (Original) A computer program as claimed in claim 20 wherein the circuit is an integrated circuit.

38. (Original) A computer program as claimed in claim 37 wherein the integrated circuit is an application specific integrated circuit.

39. (New) A method of replacing standard cells with high speed cells in the design of a circuit using a computer program, said application specific integrated circuit design comprising a plurality of high speed cells and a plurality of standard cells, said high speed cells and standard cells being arranged to form a plurality of paths on said application specific integrated circuit, said method comprising the steps of:

timing said plurality of paths

identifying paths for which timing targets are not met;

upgrading cells occurring on said identified paths to high speed cells.

40. (New) The method of claim 39, wherein:

the paths for which timing targets are not met belong to a first set of paths;

the first set of paths is determined from a second set of paths; and

the second set of paths is changed to include an increased number of paths if the paths for which timing targets are not met number less than a specified number of paths.